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(54) **INTERPOSER STRUCTURE AND MANUFACTURING METHOD THEREOF**

(71) Applicant: **UNITED MICROELECTRONICS CORPORATION**, Hsinchu (TW)

(72) Inventor: **Chien-Li Kuo**, Hsinchu (TW)

(73) Assignee: **UNITED MICROELECTRONICS CORPORATION**, Hsinchu (TW)

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H01L 23/498	(2006.01)
H01L 23/532	(2006.01)
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CPC ***H01L 21/486*** (2013.01); ***H01L 23/147*** (2013.01); ***H01L 23/49827*** (2013.01); *H01L 23/525* (2013.01); *H01L 23/53238* (2013.01)

(58) **Field of Classification Search**

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See application file for complete search history.

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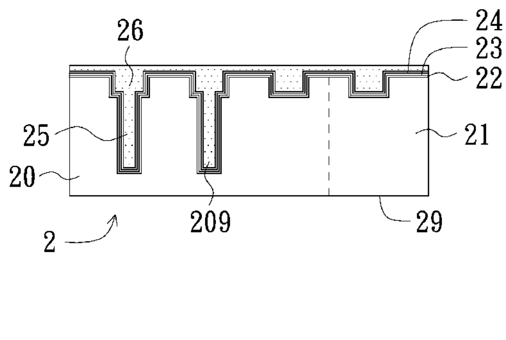
Primary Examiner — Calvin Lee

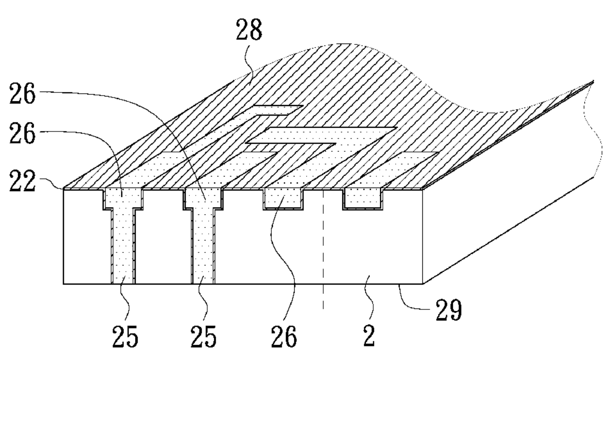
(74) *Attorney, Agent, or Firm* — Ding Yu Tan

(57) **ABSTRACT**

An interposer structure including a semiconductor substrate, a plurality of shallow trenches, a plurality of deep trenches and a plurality of metal damascene structures is provided. The semiconductor substrate has a first surface and a second surface opposite to each other. The shallow trenches are formed on the first surface in both of a first area and a second area of the semiconductor substrate and correspondingly a plurality of respective openings are formed on the first surface. The deep trenches extend from at least one of the shallow trenches toward the second surface in the second area and correspondingly a plurality of respective openings are formed on the second surface. The metal damascene structures are filled in both of the shallow trenches and the deep trenches. A manufacturing method for the aforementioned interposer structure is also provided.

5 Claims, 3 Drawing Sheets





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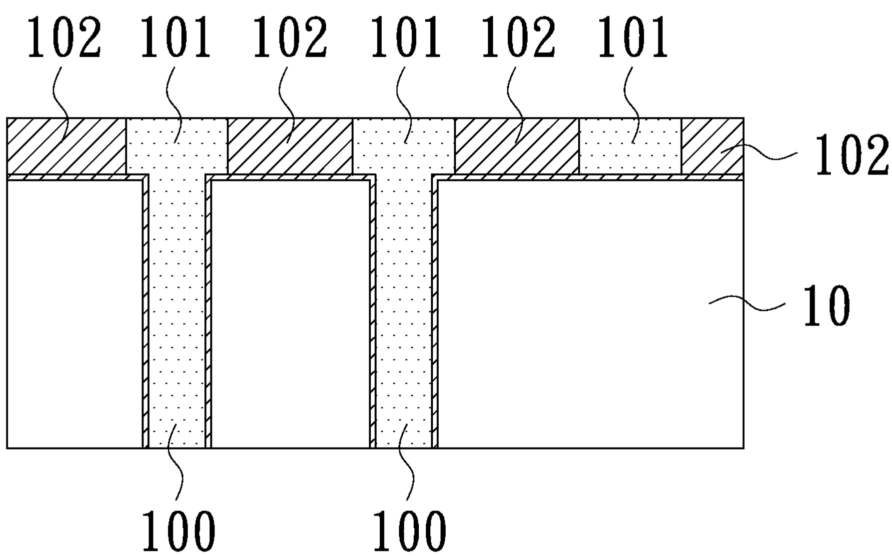

FIG. 1 (Prior Art)

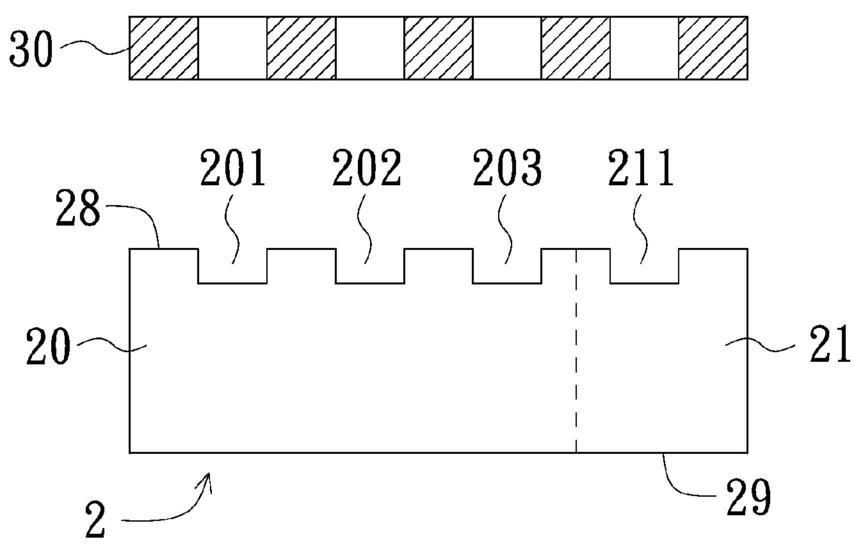
30
201
202
203
211
28
20
21
2
29

FIG. 2A

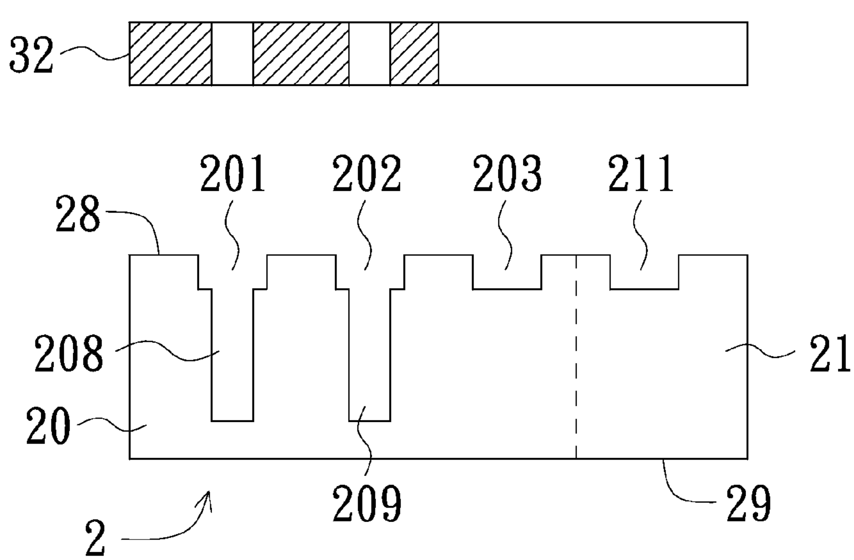
32
201
202
203
211
28
208
20
21
209
2
29

FIG. 2B

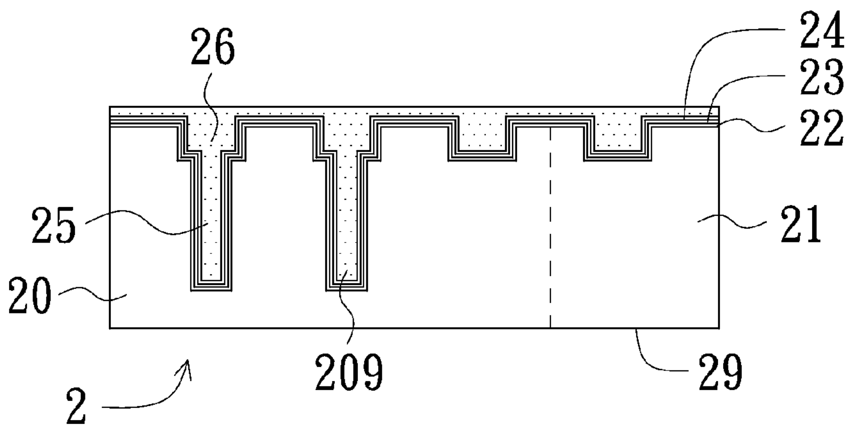

FIG. 2C

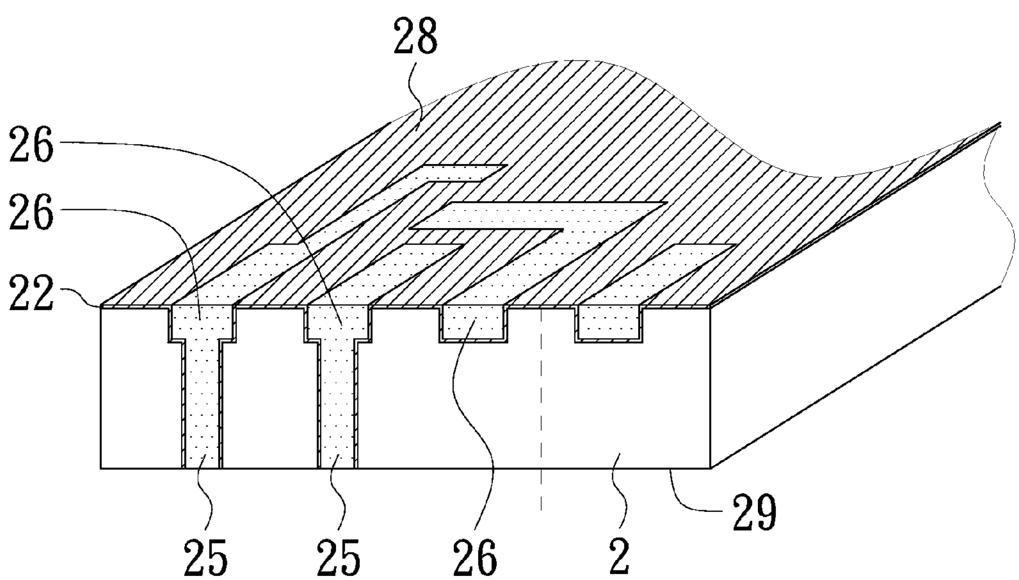

FIG. 2D

INTERPOSER STRUCTURE AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

The present invention relates to a manufacturing method for an interposer structure, and more particularly to a manufacturing method for an interposer structure by using fewer masks. The present invention also relates to an interposer structure manufactured by the method.

BACKGROUND OF THE INVENTION

Through-Silicon Via "(hereinafter referred to as TSV) is a 3D packaging technology capable of stacking a plurality of chips vertically in a manner like a sandwich. In order to have a higher finesse of chip stack, silicon interposer is accordingly developed.

FIG. **1** is a schematic cross-sectional view of a common silicon interposer structure known in prior art. As shown, a plurality of TSV structures **100** (herein in FIG. **1** is exemplified by two TSV structures **100** only) are formed in a silicon substrate **10**, and a dielectric layer **102** and a re-distribution layer (hereinafter referred to as RDL) **101** with specific patterns are formed on one side of the silicon substrate **10**. Specifically, the TSV structure **100** is used to provide a via so that the components and/or chips (not shown) disposed on top and bottom of the silicon substrate **10** can have an electrical connection to each other; and the RDL **101** is used to redistribute I/O pads and thereby enabling the related chips to apply in various component modules.

In the related art, however, the formation of the TSV structures **100** in the silicon interposer is realized by using three masks. Specifically, a first mask is used for the formation of a plurality of shallow trenches on a surface of the silicon substrate **10**, wherein these shallow trenches will be used as alignment marks for the follow-up manufacturing process. Next, a second mask, aligned with the aforementioned alignment marks, is used to define a plurality of deep trenches of the TSV structures **100**. After the deep trenches are formed by performing one or more etching processes, the TSV structures **100** for electrically connecting the components and/or chips disposed on top and bottom of the silicon substrate **10** are formed by performing a metal filling and at least one planarization process to the deep trenches. Then, a dielectric layer is formed on the substrate **10** and a third mask is used to form trenches for the RDL **101**. After the trenches for the RDL are formed, a metal filling and at least one planarization process are performed to finish fabricating of the RDL **101**. Therefore, at least three masks and multiple metal filling/planarization processes are required for the formation of the TSV structures **100** and the RDL **101** as taught in prior art or conventional related art, and consequentially the conventional interposer structure has a relatively high manufacturing cost.

SUMMARY OF THE INVENTION

Therefore, one object of the present invention is to provide an interposer structure, which has a less complicated manufacturing process and a lower manufacturing cost.

In addition, another object of the present invention is to provide a manufacturing method for the aforementioned interposer structure.

The present invention provides an interposer structure, which includes a semiconductor substrate, a plurality of shallow trenches, a plurality of deep trenches and a plurality of metal damascene structures. The semiconductor substrate has a first surface and a second surface. The shallow trenches are formed on the first surface in both of a first area and a second area of the semiconductor substrate and correspondingly a plurality of respective openings are formed on the first surface, wherein each two adjacent shallow trenches are separated by a portion of the semiconductor substrate. The deep trenches are formed and extending from at least one of the shallow trenches toward the second surface in the second area and correspondingly a plurality of respective openings are formed on the second surface. The metal damascene structures are filled in the shallow trenches and the deep trenches, respectively.

The present invention also provides a manufacturing method for an interposer structure. The manufacturing method includes steps of: providing a semiconductor substrate having a first surface and a second surface opposite to each other; performing, with using a first mask, a first patterning process on the first surface to form a plurality of shallow trenches in both of a first area and a second area of the semiconductor substrate; performing, with using a second mask and using the shallow trenches in the first area as alignment marks, a second patterning process through at least one of the shallow trenches in the second area to form a plurality of deep trenches extending from the at least one shallow trench toward the second surface; and performing a metal filling process and at least one planarization process to form a plurality of metal damascene structures in the shallow trenches and the deep trenches.

In summary, by using fewer masks, the manufacturing method for an interposer structure of the present invention has a less complicated manufacturing process; and correspondingly the interposer structure manufactured by the aforementioned method has lower cost.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

FIG. **1** is a schematic cross-sectional view of a silicon interposer structure in prior art; and

FIGS. **2**A~**2**D are schematic views illustrating a manufacturing process of a silicon interposer structure in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of preferred embodiments of this invention are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

FIGS. **2**A~**2**D are schematic views illustrating a manufacturing process for a silicon interposer structure in accordance with an embodiment of the present invention. First, as shown in FIG. **2**A, a substrate **2** having a first surface **28** and a second surface **29** opposite to each other is provided. By defining a first resist pattern (not shown) through performing a first lithography process on the silicon substrate **2** with using a first mask **30** and then performing an etching process with the first defined resist pattern as etching mask, a plurality of shallow trenches (herein the shallow trenches **201**, **202**, **203** and **211** are exemplified in FIG. **2**A) are formed. For illustrative purposes only, the first mask **30** is used with a positive photoresist layer (not shown), but it is not intended to limit the present invention. The first mask **30** includes shaded regions and unshaded regions, and only the latter allow light to pass through. After being exposed to an intense light, exposed portions of the positive photoresist layer corresponding to the unshaded regions are soluble to the developer and removed, while unexposed portions of the positive photoresist layer corresponding to the shaded regions are insoluble to the developer and remained intact to protect portions of the first surface **28** in the follow-up etching process. Therefore, the other portions of the first surface **28** which are not protected by the remaining photoresist layer will be etched through. Accordingly, the shallow trenches **201**, **202**, **203** and **211** are formed on the silicon substrate **2** and correspondingly the silicon substrate **2** has a respective number of openings formed on the first surface **28** thereof; wherein it is to be noted that each two adjacent shallow trenches **201**, **202**, **203**, **211** in this embodiment are configured be separate portions of the silicon substrate **2**. Specifically, the shallow trench **211** located in a scribe-line area **21** is used as a mask alignment mark for the follow-up manufacturing process. The rest of the shallow trenches **201**, **202** and **203** are located in a component area **20**, and are being used for the RDL in the follow-up manufacturing process. In addition, it is understood that the aforementioned lithography process and etching process together may be referred as a patterning process.

Next, by defining a second resist pattern (not shown) through performing a second lithography process on the silicon substrate **2** with using a second mask **32** and then performing an etching process with the defined second resist pattern and using the shallow trench **211** in the scribe-line area **21** as a mask alignment mark, a plurality of deep trenches (herein the deep trenches **208**, **209** are exemplified in FIG. **2**B) are formed under some or all of the shallow trenches **201**, **202** as illustrated in FIG. **2**B. The deep trenches **208**, **209** extend from the shallow trenches **201**, **202** toward the second surface **29** of the semiconductor substrate **2**. The function of the second mask **32** and the related manufacturing processes are similar to that of the first mask **30**, and no redundant detail is to be given herein.

Next, by performing a metal filling process and at least one planarization process for both of the shallow trenches and the deep trenches, a plurality of metal damascene structures for all the aforementioned trenches are formed, respectively. The metal filling process may include the following steps: forming a liner oxide layer **22** in each one of the shallow trenches **201**, **202**, **203** and the deep trenches **208**, **209**; forming a barrier layer **23** on a surface of the liner oxide layer **22**; forming a seed layer **24** on a surface of the barrier layer **23**; and forming a metal layer on a surface of the seed layer **24**. Thus, a TSV structure **25** and a respective RDL **26** are formed as illustrated in FIG. **2**C. Sometimes, the liner oxide layer **22**, the barrier layer **23**, the seed layer **24** and the metal layer are also formed in the shallow trench **211** in the scribe-line area **21** along with other trenches. However, the present invention is not limited to this structural configuration, and the stack layers may or may not be formed in the shallow trench **211**, which is previously used as a mask alignment mark, according to different applications. In this embodiment, it is understood that the substrate **2** may be other known type of semiconductor substrate; the liner oxide layer **22** may be made of any insulating material such as SiN, SiON, SiC, SiCN, SiO_2 or a combination thereof; the material of the barrier layer **23** may be Ti, TiN, Ta, TaN or a combination thereof; the seed layer **24** may be a copper seed layer; and the metal layer for both the TSV structure **25** and the RDL **26** may be made of copper. In addition, the liner oxide layer **22** may be manufactured by thermal oxidation/nitridation method or chemical vapor deposition (CVD) and is used as an isolation layer for both of the TSV structure **25** and the RDL **26**.

Then, by performing at least one planarization process on the silicon substrate **2** together with the metal layer for both the TSV structure **25** and the respective RDL **26**, a silicon interposer structure as illustrated in FIG. **2**D is formed. In one embodiment, the planarization process may comprise a chemical-mechanical polishing (CMP) process mainly for polishing the metal (Cu) layer and another CMP process for polishing the barrier layer **23**. In another embodiment, the planarization process may only comprise a CMP process mainly for polishing the metal (Cu) layer. Specifically, by performing a planarization on the first surface **28** of the silicon substrate **2**, the metal layer filled in the shallow trenches **201**, **202** and **203** forms the RDL **26**. It is to be noted that the liner oxide layer **22** on the first surface **28** of the silicon substrate **2** may be polished to be completely removed; or, there may be still a portion of the liner oxide layer **22** remaining on the first surface **28** of the silicon substrate **2** for a specific purpose. In addition, by performing at least one thinning or grinding or planarization process on the second surface **29** of the silicon substrate **2**, the metal layer filled in the deep trenches **208**, **209** forms the TSV structure **25**; wherein each one of the TSV structures **25** has a corresponding opening on the second surface **29**. Thus, compared with the prior art, the present invention has less patterning processes.

Based on the concept of the present invention, it is understood that the formation of the shallow trenches and the deep trenches may have a reverse order. The deep trenches instead of the shallow trenches may be formed in the scribe-line area and used as the mask alignment marks for the formation of the shallow trenches in the component area. However, because the deep trench has a relatively large depth, it is to be noted that using the shallow trenches as mask alignment marks is a preferred option since more effort is required in the wafer cutting process if the deep trenches are formed in the scribe-line area.

Furthermore, it is understood that another one or more re-distribution layers may be stacked sequentially on a surface of the re-distribution layer **26** if necessary, and no redundant detail is to be given herein.

In summary, by using fewer masks, the manufacturing method for an interposer structure of the present invention has a less complicated manufacturing process; and correspondingly the interposer structure manufactured by the aforementioned method has lower cost.

While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. An silicon interposer structure, comprising:

a semiconductor silicon substrate comprising a first surface and a second surface opposite to each other;

a plurality of shallow trenches formed on the first surface in a first area and a second area of the semiconductor silicon substrate, respectively, and a plurality of respective openings are correspondingly being formed on the first surface, wherein each two adjacent shallow trenches are separated by a portion of the semiconductor silicon substrate;

a plurality of deep trenches formed and extending from at least one of the shallow trenches toward the second surface in the second area of the silicon substrate and a plurality of respective openings being correspondingly formed on the second surface; and

a plurality of metal damascene structures filled in the shallow trenches and the deep trenches, wherein the shallow trenches formed in the first area are used as a mask alignment mark for the formation of the deep trenches.

2. The silicon interposer structure according to claim **1**, wherein the metal damascene structures filled in the shallow trenches and the deep trenches comprises:

a liner oxide layer formed on a surface of the shallow trenches and the deep trenches;

a barrier layer formed on a surface of the liner oxide layer;

a seed layer formed on a surface of the barrier layer; and

a metal layer formed on a surface of the seed layer.

3. The silicon interposer structure according to claim **2**, wherein the liner oxide layer is made of an insulating material of SiN, SiON, SiC, SiCN, SiO2 or a combination thereof; the barrier layer is made of Ti, TiN, Ta, TaN or a combination thereof; the seed layer is a copper seed layer; and the metal layer is a copper layer.

4. The silicon interposer structure according to claim **2**, wherein the metal damascene structures filled in the shallow trenches in the second area form a re-distribution layer (RDL).

5. The silicon interposer structure according to claim **2**, wherein the metal damascene structures filled in the deep trenches form a through-silicon via (TSV) structure.

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